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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/152,266	09/14/1998	ERIC R. CAMPBELL	540-127	8971

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NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
PHAM, THOMAS K	
ART UNIT	**PAPER NUMBER**
2121	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental Notice of Allowability	Application No. 09/152,266	Applicant(s) CAMPBELL ET AL.	
	Examiner Thomas K. Pham	Art Unit 2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 4/15/2005*.

2. ☒ The allowed claim(s) is/are *2-19 and 22-56*.

3. ☒ The drawings filed on *12 November 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 09/14/1998
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

RJ

Notice to Applicants

1. This supplemental action is for the purpose of correcting the missing examiner's initials on the IDS submitted on 09/14/1998 on the two documents listed under "OTHER DOCUMENTS" of the PTO-1449.

Reasons for Allowance

2. Claims 2-19 and 22-56 are allowed.

3. The following is an examiner's statement of reasons for allowance:

Relating to claims 2-16 and 39-56:

Jennings et al. (USPN 4,796,178) discloses a special purpose processor responsible as a task control mechanism for maintaining a queue of ready or available processes according to an assigned priority so that any of a plurality of processors may be allocate to the tasks upon available. The mechanism also computes task priorities as new tasks are entered or removed from the queue.

And Breuninger (European Patent No. EP 0 266 065) teaches a programmable sequence generator comprising a combinatorial logic matrix and an on-chip timer having count lines couples as inputs to the logic matrix. The combinatorial logic functions may be programmed into the matrix having as variables external inputs, a count number represented by the count lines and internal inputs fed back from the outputs of the logic matrix.

Jennings et al. and Breuninger do not teach a modular design comprised of an assembly of design tiles, wherein each tile defines a building block having logic and

connections, the tiles interconnected to form a two-dimensional array of n rows and m columns which realizes an overall functionality for the integrated circuit, wherein each of the n rows of tiles includes a series of stim-wait circuits and provides the control logic for one of n schedulable activities and each of the m columns of tiles is arranged to operate one or any of the stim-wait circuits in that column to a stimmed condition.

Relating to claims 17-19, 22-35 and 38:

Simpson (USPN 5,469,549) discloses a multi-processing computer system with multiple computing units, wherein each unit includes a processor linked to a private memory via a private data bus. The computing units are linked with one another via respective separate independent shared memory area that controlled by a communications controller to provide full asynchronous two-way communication route.

Simpson does not teach a set of stim-wait circuits for each activity which incorporates a next activity logic to select the next activity to be run on the associated processor dependant on the states of the stim-wait channels during execution of the activities; and other limitations related to these features in combination with the remaining elements and features of the claimed invention.

Relating to claims 36-37:

Perotto et al. ("An 8-bit Multitask Micropower RISC Core" August 1994, IEEE Journal of Solid State) discloses a multitask micropower RISC core including a hardware scheduler handles up to four separate tasks in a pseudo-parallel way where the tasks or context switching perform at the instruction level. Upon completion of a task, the processor goes in sleep-mode and awaits for the next task.

While the control variables of Perotto et al. are static at initialization to configure the processor for a specific application, Perotto et al. does not teach the control variables for controlling activities are dynamically update as the activities execute and interact; and other limitations related to these features in combination with the remaining elements and features of the claimed invention.

None of these references taken either alone or in combination discloses a method and device for use as a scheduler of activities to be run on an associated processor having all the claimed features of applicant's instant invention, specifically including: a modular design comprised of an assembly of design tiles, wherein each tile defines a building block having logic and connections, the tiles interconnected to form a two-dimensional array of n rows and m columns which realizes an overall functionality for the integrated circuit, wherein each of the n rows of tiles includes a series of stim-wait circuits and provides the control logic for one of n schedulable activities and each of the m columns of tiles is arranged to operate one or any of the stim-wait circuits in that column to a stimmed condition. In addition, each integrated circuit comprising a set of stim-wait circuits for each activity which incorporates a next activity logic to select the next activity to be run on the associated processor dependant on the states of the stim-wait channels during execution of the activities. Furthermore, the control variables for controlling activities are dynamically update as the activities execute and interact. Also, there is no motivation to combine the references to meet these limitations. It is for these reasons that applicant's invention defines over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner *Thomas Pham*; whose telephone number is (571) 272-3689, Monday to Thursday from 6:30 AM - 5:00 PM EST or contact Supervisor *Mr. Anthony Knight* at (571) 272-3687.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas Pham
Patent Examiner

July 5, 2005

Anthony Knight
Supervisory Patent Examiner
Group 3600